UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte JAMES K. FALBO, VINOD K. MALHOTRA,
PRATHEEP BALASINGAM and DONALD ZULCH

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Appeal No. 2006-1686
Application No. 10/040,055

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ON BRIEF

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Before KRASS, JERRY SMITH, and RUGGIERO, *Administrative Patent Judges.*

KRASS, *Administrative Patent Judge.*

## DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 11, 33, 37-43, and 55-99.

The invention pertains to the performance of layout beautification on an integrated circuit (IC) layout. Layout beautification is a technique for detecting and correcting a layout imperfection. A shape-based algorithm is employed by the layout beautification system.

Representative independent claim 11 is reproduced as follows:

11. A method for performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality of polygons, the method comprising applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout,

the first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection,

the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises:

a third edge, the third edge being contiguous with and substantially perpendicular to the second edge;

a fourth edge, the fourth edge being contiguous with and substantially perpendicular to the third edge; and

a fifth edge, the fifth edge being contiguous with and substantially perpendicular to the fourth edge, wherein none of the first edge, the second edge, the third edge, the fourth edge, and the fifth edge are substantially side-by-side with each other.

The examiner relies on the following reference:

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|---|---|---|
| Agrawal et al. (Agrawal) | 6,523,162 | Feb. 18, 2003 (filed Aug. 2, 2000) |

Claims 11, 33, 37-43, and 55-99 stand rejected under 35 U.S.C. § 102(e) as anticipated by Agrawal.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

A rejection for anticipation under section 102 requires that the four corners of a single prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

Taking claim 11 as exemplary, it is the examiner's position that Agrawal discloses a method for performing a layout beautification operation on an IC layout comprising a plurality of polygons at column 14, lines 16-19, column 5, lines 51-52, and column 8, lines 45-48.

Applying a first action to a first portion of the IC layout responsive to determining that a first shape associated with the first action matches the first portion of the IC layout is said to be taught at column 14, lines 24-31 of Agrawal.

The examiner contends that column 14, lines 20-23, of Agrawal disclose the claimed first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection.

The claimed feature of the second edge being contiguous with and substantially perpendicular to the first edge is said to be described in Agrawal at column 6, lines 35-37, with Figures 4a, b, and c providing examples of basic shapes.

The examiner further points to Figures 4a-4c, 5a-5d, 6a-6e, 7a-7c, particularly Figure 4b of Agrawal for a teaching of the first shape comprising a third edge, the third edge being contiguous with and substantially perpendicular to the second edge.

A fourth edge, contiguous with and substantially perpendicular to the third edge, is said to be taught by Agrawal in Figures 4a-4c, 5a-5d, 6a-6e, 7a-7c, and particularly in Figure 4c, wherein the fourth edge E434 is contiguous and substantially perpendicular with the third edge E433.

Finally, the examiner asserts that Agrawal discloses a fifth edge being contiguous with and substantially perpendicular to the fourth edge, wherein none of the first edge, the second edge, the third edge, the fourth edge, and the fifth edge are substantially side-by-side with each other, at column 6, lines 44-51, column 17, lines 10-21, and in Figures 4a-4c, 5a-5d, 6a-6e, 7a-7c, in particular, Figure 4c, wherein the fifth edge E435 is contiguous and substantially perpendicular with the fourth edge E434.

Appellants' position is that while Agrawal teaches applying layout processing to an IC layout using a shape-based identification system, Agrawal does not disclose or suggest layout beautification or a layout imperfection as recited in the instant claims.

Moreover, appellants contend that Agrawal fails to recognize the problem of layout imperfections and the benefits of applying shape identification to layout beautification and that it is appellants who "have advantageously recognized the problem presented by layout imperfections, which are electrically correct and yet adversely affect layout printability or device performance" (principal brief-page 16).

Appellants also argue that the examiner's "picking and choosing" from various shapes in various figures of Agrawal is inappropriate and that Agrawal does not describe the claimed first shape having the recited first, second, third, fourth, and fifth edges (principal brief-page 17).

Thus, appellants conclude that Agrawal fails to disclose or suggest layout beautification, layout imperfection, and the recited edge configuration.

When the examiner responds that the layout beautification is merely in a non-limiting preamble, since the claimed steps do not include layout beautification or layout imperfections, appellants

argue that this is a new ground of rejection because appellants have been arguing the layout beautification and layout imperfection limitations throughout the prosecution of the case and the examiner has only in the answer concluded that such limitations appear in the non-limiting preamble.

With regard to independent claim 11, it is true that Figure 4c of Agrawal shows a first shape comprising the first, second, third, fourth and fifth edges, as claimed.

However, claim 11 also requires that the first shape be "configured to match a first type of layout imperfection." The examiner says that this limitation is described in Agrawal at lines 20-23 of column 14. The reference portion identified is within claim 1 of the patent reference and recites:

> accessing a definition of a first shape comprising a first edge and a second edge coupled in accordance with a first plurality of properties associated with the first shape.

This portion of Agrawal mentions nothing about "layout imperfection." In fact, Agrawal appears to having nothing to do with layout imperfections or "layout beautification," as

described and claimed by appellants. Agrawal is concerned with layout processing and uses a shape-based layout processing scheme for IC layout modifications.

When argued as such by appellants, the examiner's only response is that the layout beautification method of the instant invention is only in a "non-limiting preamble" (answer-page 5). Thus, the examiner does not deny that Agrawal fails to disclose a "layout beautification" method, as that term is described by appellants. The examiner contends that the instant specification does not distinguish such a "layout beautification" method from optical proximity correction (OPC) modification and design rule checking (DRC). Accordingly, the examiner appears to equate Agrawal's OPC and DRC operations with the claimed "layout beautification" operation.

We disagree with the examiner. While the specification could have been clearer in explaining, or defining, "layout beautification," paragraphs [0003] through [0006] of the specification do describe how OPC and DRC are automated tools which have been used to perform various operations on an IC

layout, but that while these tools enable the accurate creation of IC layouts, the rules embodied in these tools may result in "layout imperfections." Thus, while the results of the automated tools may be electrically correct and optically correct, the polygons that make up the actual IC layout might include unintended irregularities, or "layout imperfections" which may adversely affect layout printability or device performance. The specification also explains how "layout beautification" is a technique for detecting and correcting such layout imperfections.

Thus, it does appear to us that the instant specification does, in fact, at least distinguish "layout beautification" (a technique for detecting and correcting layout imperfections) from OPC and DRC (automated tools used to perform various operations on an IC layout to accurately create the IC layouts). With this distinction in mind, while it is clear that Agrawal describes OPC and DRC tools, it is not clear to us that Agrawal describes the claimed layout beautification and layout imperfections.

We also disagree with the examiner's attempt to disassociate the claim preamble from the body of the claim. The performance of "layout beautification" is recited in the preamble of claim 11, but this operation clearly relates to the configuration of the first shape "to match a first type of layout imperfection" recited at lines 9-10 of the claim.

Since Agrawal fails to describe any "layout imperfections" and/or "layout beautification," as described and claimed by appellants, and the examiner has not convinced us of any equivalents in Agrawal to these recited features, we will not sustain the rejection of claim 11 under 35 U.S.C. § 102(e).

We also will not sustain the rejection of claims 33, 37, 38, 39-43, 55-64, 72-90, and 96-99 under 35 U.S.C. § 102(e) as these claims also recite a layout beautification technique.

Claims 65-71 and 91-95 do not recite a layout beautification technique explicitly, but they do recite the correction of layout imperfections and describe how corrective action to the layout is

to be taken based on shape analysis. Since such correction techniques are not described or suggested by Agrawal, we also will not sustain the rejection of claims 65-71 and 91-95 under 35 U.S.C. § 102(e).

The examiner contends that certain non-critical features of Agrawal are to be read as the claimed imperfections (answer-page 6), referring to column 3, lines 4, 5, and 12-16 of Agrawal. To whatever extent these non-critical features may be considered a "layout imperfection" (and it is not clear to us that such non-critical features are such imperfections), Agrawal is clearly referring to OPC correction in this portion and the claimed layout imperfections must be of the type that may adversely affect layout printability or device performance, but may not necessarily be defects in the sense that the IC layout may still be electrically correct (see page 2 of the instant specification for the required definition of "layout imperfection"). The "layout imperfections" recited in the instant claims result from the interaction of the rules embodied in such tools as OPC. The layout imperfections are not something which may be corrected by

OPC (see page 1 of the instant specification). Therefore, the description at column 3, lines 4, 5, and 12-16, of Agrawal cannot describe the claimed "layout imperfections."

Because Agrawal has not been shown to our satisfaction to describe the "layout beautification" and "layout imperfection" as claimed and described in the instant specification at paragraphs [0003] through [0006], which is the meaning we ascribe to these terms in the instant claims, we have not sustained the rejection of any of the claims under 35 U.S.C. § 102(e).

We do note, in passing, however, that we are troubled by claims 11, 33, 37-43, 55-57, 59-64, and 85 because these claims, while reciting the performance of a layout beautification, do not specifically recite any actions, such as corrective actions, replacements, etc. which would actually effect such a layout beautification. As such, the claims appear to be incomplete or indefinite in some manner. However, there is no rejection under 35 U.S.C. § 112, second paragraph, before us as the examiner has apparently determined that no such problem exists.

The examiner's decision is reversed.

REVERSED

ERROL A. KRASS )
Administrative Patent Judge )
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JERRY SMITH ) BOARD OF PATENT
Administrative Patent Judge ) APPEALS AND
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) INTERFERENCES
JOSEPH F. RUGGIERO )
Administrative Patent Judge )

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BEVER HOFFMAN & HARMS, LLP
1432 CONCANNON BLVD
BLDG G
LIVERMORE, CA 94550-6006